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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/880,166	06/12/2001	Nisha D. Talagala	5181-80501	6782

7590 12/15/2004

Robert C. Kowert
Conley, Rose, & Tayon, P.C.
P.O. Box 398
Austin, TX 78767

EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/880,166	TALAGALA ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

0. This office action is in response to Applicants' Amendment of 6/10/04.

0.1 **Claims 1-54** remain pending.

0.2 The rejections and objections of record are maintained in response to Applicants' Amendment.

Response to Arguments

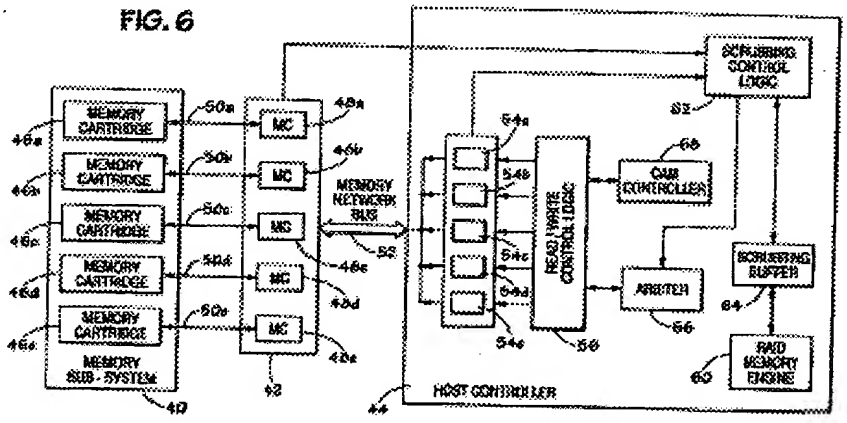
2. **Applicants' arguments** are moot in view of new ground of rejection because Applicant's arguments with respect to the rejection(s)of claim(s) 1-54 under 35 USC 103 (a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Larson et al. (US PGPUB No. 2001/0047497; filed January 26, 2000) and Davis (US Patent No. 5,819,109; October 6, 1998).

Claim Rejections - 35 USC ' 103

3. **Claims 1-54** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Larson et al.** in view of **Katz et al.** (US Patent No. 5,195,100).

As per Claims 1-54, Larson et al. substantially discloses the claimed RAID storage means (e.g., Fig. 6 and paras. 9, 26, 32, 34, 36-42) comprising: array of plural storage devices and array/disk controlling/scrubbing means for parallel data transfer/access therebetween to reconstruct data subsequent to detection of storage failure.

FIG. 6



Not specifically described in detail in Larson et al. is the step of silent error detection and correction via parity/CRC/checksum means.

However silent error detection via parity/CRC/checksum means for RAID adequate operation is one of the desiderata of RAID design. For example, **Katz et al.,** in an analogous art, discloses RAID *architecture* in Figs. 6-7, and col. 1 line 7 – col. 18 line 16.

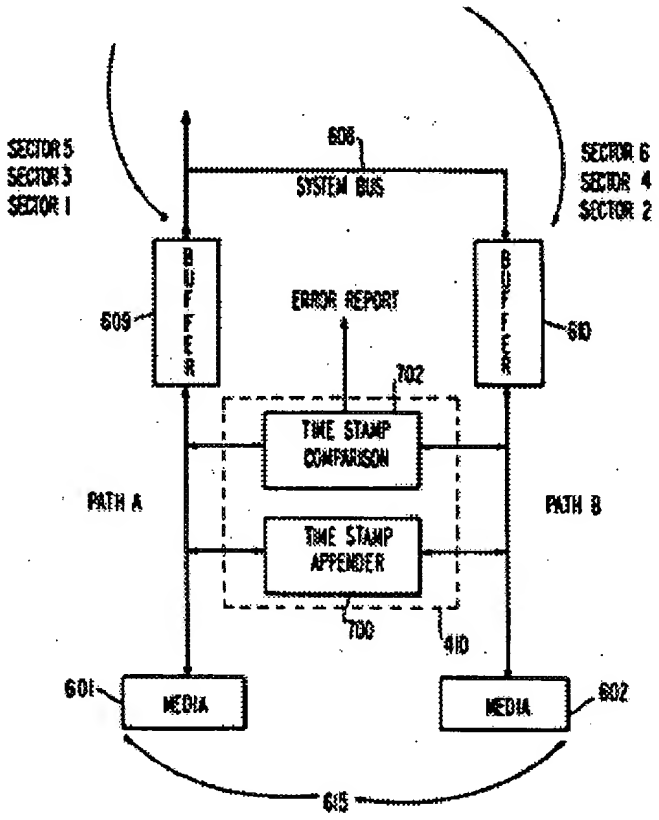


FIG.7

wherein plural fields are provided for data error checking via CRC, e.g., 3^{d} field for RAID 310 and 6th field for RAID 504 along with means for time-stamping for tracking RAID status, e.g., device 601. Such data error checking is effected and configured for local or system-wide operation based on stimuli from either the system/extent/array controller or the local/RAID/disk

controller. Corrective steps are taken in col. 6 line 35 et seq., e.g., via RS code spread across plural disks for data reconstruction in col. 6 line 62 in a manner equivalent to the claimed invention, e.g., "*a **Reed Solomon** coding algorithm is used to calculate the check data that is stored on the check drives. In a particularly preferred embodiment this **check data is distributed across several physical disk drives in a striped manner** like that of the previously described RAID level 5 architecture. A stripe comprises corresponding sectors across a set of disk drives, some of which sectors contain mass storage data and others of which sectors contain check data for the mass storage data sectors within the stripe. **A stripe may be one or more sectors deep**. Such stripes on a set of disks are grouped into one or more of what is hereafter referred to as redundancy groups. In this arrangement the physical devices comprising the **check drives for a particular stripe varies from stripe to stripe**. The widths of the stripes (i.e., the number of physical storage devices spanned by each stripe) are equal within a redundancy group.*"

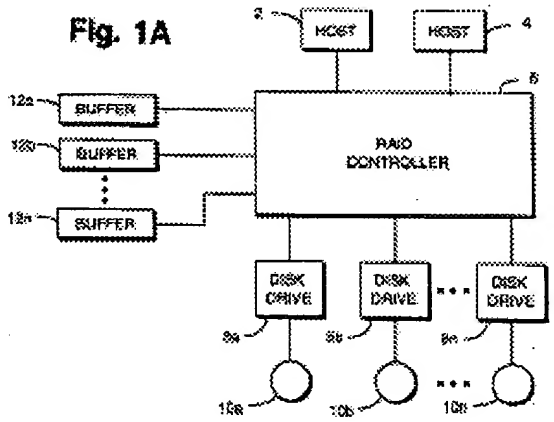
Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the RAID of **Larson et al.** by including therein silent error detection via parity/CRC/checksum means as taught by **Katz et al.,** because such modification would provide the RAID disclosed in **Larson et al.** with a technique wherein "*The third field is the CPU data block 503 as sent from or to CPU bus or channel 319. The fourth field is a CRC code 504 appended by device controller 302 on transmission to RAID controller 310 and checked by RAID controller 310. CRC code 504 is checked again and stripped by device controller 302 on receipt from RAID controller 310. Inclusion of this field 504 allows the disk storage system to detect random data errors occurring on the bus between the device controller and the RAID controller. The sixth field is a CRC code 506 appended by the RAID controller on a write operation and checked and stripped by the RAID controller on a read operation. As previously described, inclusion of this field allows the disk storage system to detect random bit errors occurring within the data block covering the*

additional device controller CRC 504 and time stamp 505 fields, during transmission between the disk and the RAID controller." {See **Katz et al.,** col. 3 lines 30-41, col. 7 line 48 et seq.}

3.1 Claims 1-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis in view of **Katz et al.** (US Patent No. 5,195,100).

As per Claims 1-54, Davis substantially discloses the claimed RAID storage means (e.g., Figs. 1a and 2 and related description at col. 1 line 18 et seq.) comprising: array of plural storage devices and array/disk controlling/scrubbing means, e.g., in Fig. 2, for parallel data transfer/access therebetween to reconstruct data subsequent to detection of storage failure.

Fig. 1A



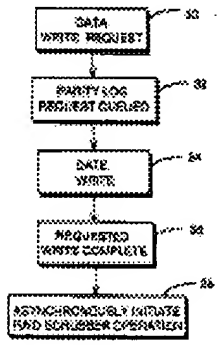


Fig. 2

Not specifically described in detail in Davis is the step of silent error detection and correction via parity/CRC/checksum means.

However silent error detection via parity/CRC/checksum means for RAID adequate operation is one of the desiderata of RAID design. For example, **Katz et al.,** in an analogous art,

discloses RAID *architecture* in Figs. 6-7, and col. 1 line 7 – col. 18 line 16.

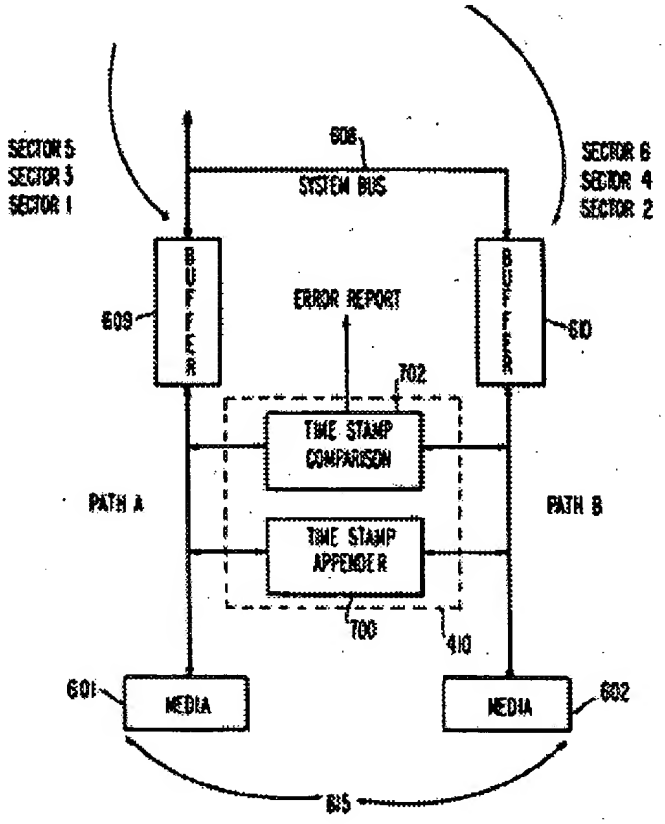


FIG.7

wherein plural fields are provided for data error checking via CRC, e.g., 3[d] field for RAID 310 and 6[th] field for RAID 504 along with means for time-stamping for tracking RAID status, e.g., device 601. Such data error checking is effected and configured for local or system-wide operation based on stimuli from either the system/extent/array controller or the local/RAID/disk controller. Corrective steps are taken in col. 6 line 35 et seq., e.g., via RS code spread across plural disks for data reconstruction in col. 6 line 62 in a manner equivalent to the claimed invention, e.g., "*a **Reed Solomon** coding algorithm is used to calculate the check data that is stored on the check drives. In a particularly preferred embodiment this **check data is distributed across several***

physical disk drives in a striped manner *like that of the previously described RAID level 5 architecture. A stripe comprises corresponding sectors across a set of disk drives, some of which sectors contain mass storage data and others of which sectors contain check data for the mass storage data sectors within the stripe.* ***A stripe may be one or more sectors deep.*** *Such stripes on a set of disks are grouped into one or more of what is hereafter referred to as redundancy groups. In this arrangement the physical devices comprising the* ***check drives for a particular stripe varies from stripe to stripe.*** *The widths of the stripes (i.e., the number of physical storage devices spanned by each stripe) are equal within a redundancy group."*

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the RAID of **Davis** by including therein silent error detection via parity/CRC/checksum means as taught by **Katz et al.,** because such modification would provide the RAID disclosed in **Davis with** a technique wherein "*The third field is the CPU data block 503 as sent from or to CPU bus or channel 319. The fourth field is a CRC code 504 appended by device controller 302 on transmission to RAID controller 310 and checked by RAID controller 310. CRC code 504 is checked again and stripped by device controller 302 on receipt from RAID controller 310. Inclusion of this field 504 allows the disk storage system to detect random data errors occurring on the bus between the device controller and the RAID controller. The sixth field is a CRC code 506 appended by the RAID controller on a write operation and checked and stripped by the RAID controller on a read operation. As previously described, inclusion of this field allows the disk storage system to detect random bit errors occurring within the data block covering the additional device controller CRC 504 and time stamp 505 fields, during transmission between the disk and the RAID controller.*" {See **Katz et al.,** col. 3 lines 30-41, col. 7 line 48 et seq.}

Conclusion

4. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Customer Services, 220 20th Street S., Crystal Plaza II, Lobby, Room 1B03, Arlington, VA 22202.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
12/12/04